

What is claimed is:

- SUB C1
- 1 1. A capacitor comprising:
2 a plurality of conductive layers embedded in a dielectric; and
3 a plurality of vias coupling at least two of the plurality of conductive layers to a
4 plurality of connection sites.
 - 1 2. The capacitor of claim 1, wherein the capacitor has a thickness of between about
2 .5 millimeter and about 1 millimeter.
 - 1 3. The capacitor of claim 2, wherein the capacitor has a capacitance of between
2 about 20 and about 30 microfarads.
 - 1 4. The capacitor of claim 1, wherein the plurality of controlled collapse chip
2 connection sites have a pitch of between about 100 and about 500 microns.
 - 1 5. The capacitor of claim 1, wherein the plurality of vias are plated through holes.
 - 1 6. A capacitor comprising:
2 a plurality of first conductive layers;
3 a plurality of second conductive layers interlaced with the plurality of first
4 conductive layers;
5 a number of surfaces having a plurality of connection sites operable for coupling
6 the capacitor to a substrate using a controlled collapse chip connection (C4); and
7 a plurality of vias coupling the plurality of first conductive layers and the plurality
8 of second conductive layers to at least two of the plurality of connection sites.
 - 1 7. The capacitor of claim 6, wherein each of the plurality of first conductive layers is
2 fabricated from a tungsten paste.
- SUB B1
- SUB B2
- SUB C1

SUB
C1

SUB
B3

1 8. The capacitor of claim 6, wherein the number of surfaces is two.

1 9. A capacitor comprising:
2 a multilayered capacitor having a number of outer surfaces; and
3 a number of pads located on at least two of the number of outer surfaces wherein
4 at least two of the number of pads are capable of being coupled to a substrate using a
5 solder bump.

1 10. The capacitor of claim 9, wherein the multilayered capacitor includes a number of
2 parallel conductive layers and the number of pads are coupled to the number of parallel
3 conductive layers through vias.

1 11. The capacitor of claim 10, wherein the number of conductive layers is greater than
2 about 50.

1 12. The capacitor of claim 11, wherein the number of pads is greater than about 4000.

1 13. A system comprising:
2 a die including an electronic system;
3 a capacitor located less than about .1 millimeter from the die and coupled to the
4 die, the capacitor is capable of decoupling a power supply connection at the die without
5 additional capacitors located external to the die; and
6 a dielectric layer located between the capacitor and the die.

1 14. The system of claim 13, wherein the dielectric layer has a thickness of between
2 about .05 millimeters and about .1 millimeters.

1 15. A system comprising:
2 a first die;
3 a second die; and

4 a capacitor having a first surface having a controlled collapse chip connection
5 coupled to the first die and a second surface having a controlled collapse chip connection
6 coupled to the second die.

1 16. The system of claim 15, wherein the first die includes a processor and the second
2 die includes a communication system.

1 17. A system comprising:
2 a substrate having a surface; and
3 a capacitor having a plurality of vias coupled to a plurality of conductive layers in
4 the capacitor, the capacitor is coupled to the surface at a plurality of connection sites.

1 18. A system comprising:
2 a substrate having a first surface and a second surface;
3 a die coupled to the first surface; and
4 a capacitor having a plurality of vias coupled to a plurality of conductive layers in
5 the capacitor, the capacitor is coupled to the second surface by a controlled collapse chip
6 connection and the capacitor is electrically coupled to the die through the substrate.

1 19. The system of claim 18, wherein the die includes a processor.

1 20. The system of claim 19, wherein the die has a die surface and the capacitor has a
2 capacitor surface and the capacitor surface is located less than about .1 millimeter from
3 the die surface.

1 21. A system comprising:
2 a processor requiring at least 5 watts of power to be operable; and
3 a single multilayered single package capacitor coupled to the processor and
4 capable of decoupling a power supply from the processor.

1 22. The system of claim 21, wherein the single multilayered single package capacitor
2 is capable of being mounted on a substrate by a plurality of solder bumps.

1 23. The system of claim 22, wherein the single multilayered capacitor is capable of
2 being mounted on a substrate using a controlled collapse chip connection.

1 24. A method comprising:
2 forming a stack of a plurality of screen printed dielectric sheets;
3 forming a plurality of via holes in the stack;
4 filling at least two of the plurality of via holes with a metal slurry; and
5 co-firing the stack to form a capacitor.

1 25. The method of claim 24, further comprising:
2 coupling the stack to a substrate using a controlled collapse chip connection.

1 26. The method of claim 24, further comprising:
2 coupling a die to the substrate and to the capacitor.

1 27. A method comprising:
2 forming a capacitor having a plurality of conductive layers and a surface; and
3 forming a pattern of pads on the surface, at least one pad in the pattern of pads is
4 capable of being coupled to at least one of the plurality of conductive layers and capable
5 of being coupled to a substrate using a solder bump attachment.

1 28. The method of claim 27, further comprising:
2 coupling the capacitor to a ceramic substrate using a solder bump attachment.

1 29. A method comprising:
2 selecting a substrate having a controlled collapse chip connection capability; and

